REMARKS

Claims 2-5, 7-12, and 18 will be pending upon entry of the present amendment. Claims 1, 6, and 13-17 are being canceled. Claims 2-5 and 7-12 are being amended. Claim 18 is new.

The drawings were objected to because Figures 5-8 were not designated by a "Prior Art" legend. Enclosed are revised Figures 5-8 with the appropriate legends.

The drawings were also objected to for failing to show the "logic block consisting of full adder and full subtractor elements" recited in claim 1. Claim 1 is being rewritten as claim 18 without the recited language. Accordingly, the drawings are not be amended to show such features.

The specification was objected to for lacking an Abstract. A new abstract is being provided.

The specification was also objected to because the headings suggested in 37 CFR 1.77(b). The specification is being amended to include the relevant headings.

Claims 1, 7, and 9 were objected to for informalities and claims 1-17 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claim 1 is being rewritten as new claim 18 to address the items specifically identified by the Examiner and the numerous limitations that lacked antecedent bases. Claims 2-5 and 7-12 are being similarly amended. As such, claims 2-5, 7-12, and 18 particularly point out and distinctly claim the invention.

Claims 7-11 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,370,556 to Saramaki et al. ("Saramaki"). Claim 12 was rejected under 35 U.S.C. § 103 as being unpatentable over Saramaki.

Independent claim 7 is being amended to recite a filter in which each sequential subtractor or adder element includes a carry-out pin fed to an input of one of the sequential subtractor or adder elements of a previous one of the combinational logic blocks. In addition claim 7 recites that a sequential logic block has m delay elements for receiving respective outputs of the combinational logic blocks B0, B1, ...Bm-1 and for providing delayed outputs to respective inputs of the combinational logic blocks B1, B2, ...Bm, respectively, such that the

same delay element is used for multiplication by a factor of two and also for a carry function. Independent claim 8 is being amended similarly.

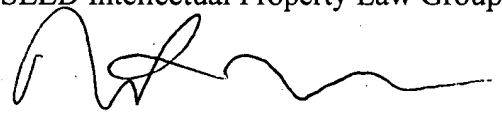
Saramaki does not teach or suggest the invention recited in claims 7-12, as amended. In particular, Saramaki does not teach or suggest the claimed arrangement in which each subtractor or adder element includes a carry-out pin that is fed to an input of one of the sequential subtractor or adder elements of a previous one of the combinational logic blocks. That feature, in combination with the delay elements providing delayed outputs to the respective inputs of the subtractor or adder elements, enables the same delay element to be used for multiplication by a factor of two and also for a carry function. Saramaki does not teach or suggest these features, as apparently recognized by the Examiner in failing to reject claims 1-6 based on Saramaki. Accordingly, claims 7-12 are in condition for allowance.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



Robert Iannucci
Registration No. 33,514

RXI:lmt

Enclosure:
Postcard
2 Sheets of Drawings (Figures. 5-8)

701 Fifth Avenue, Suite 6300
Seattle, Washington 98104-7092
Phone: (206) 622-4900
Fax: (206) 682-6031

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